REMARKS

The Applicant has filed the present Response in reply to the outstanding Official Action of April 20, 2005, and the Applicant believes the Response to be fully responsive to the Official Action for the reasons set forth below in greater detail.

At the onset, Applicant would like to note that Claims 1, 15 and 16 have been amended herewith. Claim 1 has been amended to further recite that the first quality data, second quality data, and received data are transferred as demodulated data to a control unit. Claim 15 has been amended to make the claim language consistent with an embodiment illustrated in Figure 1. Specifically, the claim has been amended to recite "a first subtracter for obtaining a first difference signal between the phase data and the delayed signal by the one symbol delaying unit on the basis of a correction signal; a second subtracter for obtaining a second difference signal between the phase data and the delayed signal by the one symbol delaying unit". Additionally, the claim has been amended to further recite that the first decoder and second decoder being in parallel with each other. Claim 16 has been amended to clarify the claim. Claim 16 is directed to the second embodiment of the invention which is illustrated in Figure 2. The amendment to Claim 16 does not add any new matter and support therefor can be found in Figure 2.

The amendments to Claims 1 and 15 do not add any new matter as such amendments are supported by the specification. For example, support can be found in Figure 1.

In the FINAL Official Action, the Examiner rejected Claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by Fukushi (U.S. Patent No. 5,793,250) (hereinafter "Fukushi").

Applicant respectfully disagrees with each and every rejection of the claims and traverses with at least the following analysis.

First, the Applicant would like to note that the Examiner appears to improperly cite different elements of the cited reference to read on the same claim features that are recited in different claims.

With respect to Claim 1, the Examiner avers that Fukushi discloses a phase modulator the selectively uses a first or second detector. Fukushi discloses two phase-distortion calculators 17 and 26 that generate a first and second quality data. Therefore, according to the Examiner, Fukushi teaches all of the claim limitations.

Applicant submits that Claim 1 is patentably different from the prior art reference. The reference fails to teach that "said first quality data, second quality data, and received data are transferred as demodulated data to a control unit", as specifically recited in Claim 1. In a disclosed embodiment, the specification describes that the first decoder transfers the upper two bits and the lower three bits as received data and quality control data to the control unit. The control unit executes a computation process on the quality data. The second decoder converts the lower three bits of its input data as quality data and transfers this data to the control unit. Therefore, both the first and second quality data and the received data are transferred to the control unit as demodulated data. The second quality data is used to drive the AFC unit.

The prior art reference does not teach these features. Specifically, in the cited prior art reference, the output of the phase-distortion calculators 17 and 26 is not transferred to the control unit as demodulated data. Several other stages of demodulation occur before the signals are even sent to the phase discriminator (phase discriminator is

not equivalent to the control unit). In fact, there is a phase distortion comparator that compares the phase distortions of the first and second detected signals to generate a resultant signal. The resultant signal is used as a control signal for the selector. In other words, the selector (switch) transfers the output of one of the detectors to the phase discriminator based upon the resultant signal, i.e., higher quality signal.

Accordingly, the reference fails to teach the claimed structural elements and function. Therefore, Claim 1 is patentably distinct from the cited reference as the reference does not teach or suggest each and every limitation of the claim.

Claims 2, 3, and 5 are patentable based upon their dependency from Claim 1 and based upon the reasons identified above.

In addition to being patentably distinct from the cited reference based upon the above-identified reasons, Claim 4 is further patentably distinct from the reference for the following additional reasons.

Fukushi fails to teach or suggest the feature of "wherein the second data generating means further generates received data on the basis of the received signal," as recited in Claim 4. In a disclosed embodiment, the first decoder generates both a second quality data 133b and a received data 133a. Fukushi does not teach that the second data generating means generates both a second quality data and a received data. In fact, the Examiner avers that the phase discriminator generates demodulated data (received data) using the output of either the first or second phase distortion calculators. The first or second phase distortion calculators solely generate a first quality data and second quality data and **not the received data**. Accordingly, the reference does not teach that second

data generating means further generates received data. Therefore, the claim is patentably distinct from the cited reference.

With respect to Claim 6, Fukushi fails to teach or suggest the features of "the second data generating means including a correcting circuit for correcting the **received signal frequency data,** and a **decoder for generating the second quality data and received data on the basis of new frequency data obtained in the correcting circuit"** as specifically claimed.

The Examiner avers that Fukushi discloses correcting the input to the second detector by way of DPL 22. However, the reference states that the PLL circuit 22 receives the angle value calculated by the angle calculator and outputs a compensated angle value taking into consideration the frequency offset. PLL circuit includes a phase adjuster. This PLL circuit is used to correct the phase and **not the received signal frequency data**. Additionally, the reference does not teach a decoder for generating the second quality data and received data. Once again, the Examiner states that the reference discloses decoding the received data output from the second detector using a phase discriminator. This is not a fair characterization of what is disclosed by the reference. As illustrated by Figure 1 of the instant applicant, the decoder outputs both the quality data and the received data. The alleged decoder (of the cited reference) does not output both quantities.

Accordingly, Claim 6 is patentably distinct.

Claim 7 is patentable for the same reason as Claim 6.

In addition to being patentably distinct from the cited reference based upon the above-identified reasons, Claim 8 is further patentably distinct from the reference based upon the following additional analysis.

Fukushi fails to teach or suggest the feature "of wherein the second quality data is used as line control data", as specifically recited in Claim 8.

The Examiner avers that the reference discloses that the output from the integrator is used to drive a switch that selects one output from two inputs to transmit the one output to the phase discriminator. Applicant respectfully disagrees with this contention. Specifically, Applicant submits that the second quality data is not output from the integrator. In fact, the Examiner admits that the coherent detector 26 outputs the second quality data. Additionally, the result of the comparison between the first output and the second output is used to drive the switch, not the second quality data.

In contrast, the claim recites that the second quality data is used as line control data. Further, in a disclosed embodiment, the specification states that the control unit 109 makes the second quality data to be a data means for line control in the portable telephone set.

Therefore, the reference does not teach all of the limitations of the claim, and Claim 8 is patentably distinct from the reference.

With respect to Claim 9, the Examiner asserts that the frequency offsets circuit elements 18 and 36 are the correcting means, as claimed. Applicant submits that the Examiner is inconsistent with his assertions regarding the correcting circuit and means. Specifically, in Claim 6 the Examiner avers that the PLL circuit 22 is the correcting

circuit and now the Examiner avers that the frequency offsets circuit elements are the correcting means.

However, Applicant submits that element 18 is just a frequency offset holder. Additionally, while element 36 subtracts a frequency offset from the phase angle difference value, the data generating means, i.e, elements 17 and 26, **do not generate quality data on the basis of new frequency data obtained in the correcting means.** The Examiner contends that elements 17 and 26 are the first and second data generating means in Claim 1, but contends that the phase discriminator is the data generating means in Claim 9. These elements are separate and distinct elements, whereas, in the claimed invention, the data generating means is a single element. The reference fails to teach the claimed structure.

Accordingly, Claim 9 is patentably distinct from the cited reference. Claims 12 and 13 are patentable for the same reason as applied to Claim 9.

Claim 14 is patentable based upon the same reason as cited above with regard to Claim 8.

In addition to being patentably distinct from the cited reference based upon the above-identified reasons, Claims 10 and 11 are further patentably distinct from the reference for the following additional reasons.

With respect to Claim 10, the Examiner incorrectly asserts that the integrator is the data generating means. Once again, the Examiner inconsistently identifies the data generating means. (Claim 1, elements 17 and 26; Claim 9, phase discriminator; Claim 10, integrator). Similarly, with respect to Claim 11, the Examiner asserts that the phase

discriminator is the data generating means. The term "data generating means" should be interpreted the same for all of the claims.

With respect to amended Claim 15, the reference fails to disclose "a first decoder for decoding the first difference signal to produce the received data and a first quality data of a reception line; and a second decoder for decoding the second difference signal to produce a second quality data of the reception line wherein the first decoder and second decoder being in parallel with each other ", as specifically recited.

The Examiner avers that Fukushi discloses an integrator 17 that calculates phase distortion and a phase discriminator to produce demodulated data. However, it is not clear from the rejection which single element is the decoder. In the claimed invention, the first decoder decodes the first difference signal to produce the received data and a first quality data. The reference fails to teach that a decoder produces both the received data and the first quality data.

Furthermore, the Examiner avers that the integrator element 19 and the second subtracter element 36 create the phase distortion data, i.e., second quality data. First, the integrators 17 and 19 are in series, whereas the first and second decoders are in parallel. Second, it is not clear from the rejection which single element is the second decoder.

Moreover, the first decoder is attached to the correction circuit whereas the second decoder is independent from the correction circuit. Neither integrator 17 nor 19 is attached to the correcting circuit.

Accordingly, Claim 15 is patentably distinct from the cited reference.

With respect to Claim 16, the cited reference does not teach the claimed digital portable telephone set including means for demodulating a received signal and

reproducing data, consisting of the recited elements. Claim 16 is directed to the second embodiment of the invention. As described in the specification, the second embodiment of the invention is designed to reduce the number of components needed for operation. The second embodiment features a simpler circuit construction. This embodiment comprises a delay unit, a subtracter, a decoder and a correcting circuit. The decoder outputs, as demodulated data, the output from the correcting circuit together with received data and quality data. As such, the reference does not teach this reduction in the number of components and, in fact, requires substantially more components. This would, therefore, increase both the cost and size of the circuit.

Accordingly, Claim 16 is patentably distinct from the cited reference.

For all the foregoing reasons, the Applicant respectfully requests the Examiner to withdraw the rejections of Claims 1-16 pursuant to 35 U.S.C. § 102(e).

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

Seth Weinfeld
Registration No: 50,929

SW:ae
Scully, Scott, Murphy & Presser
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343